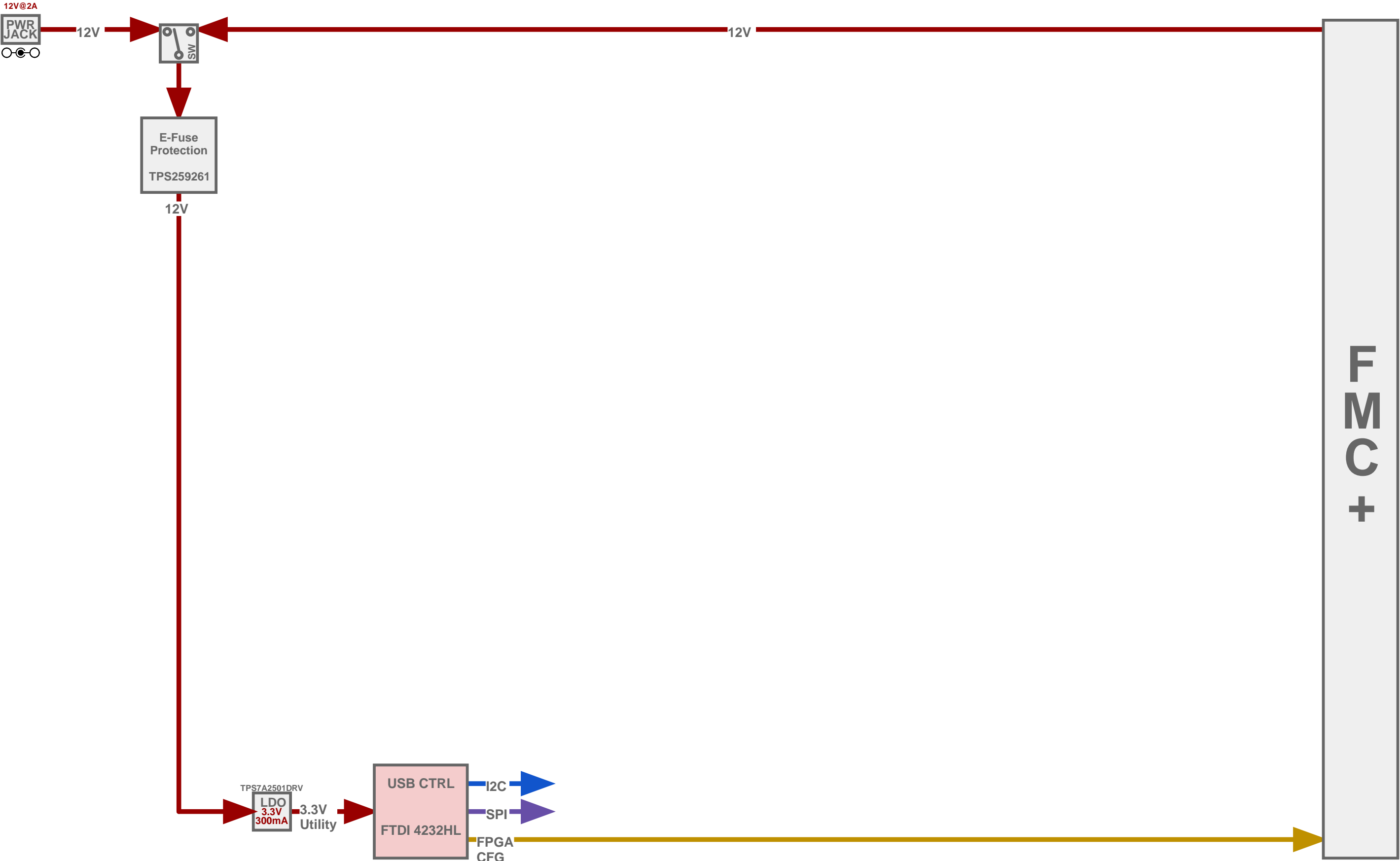


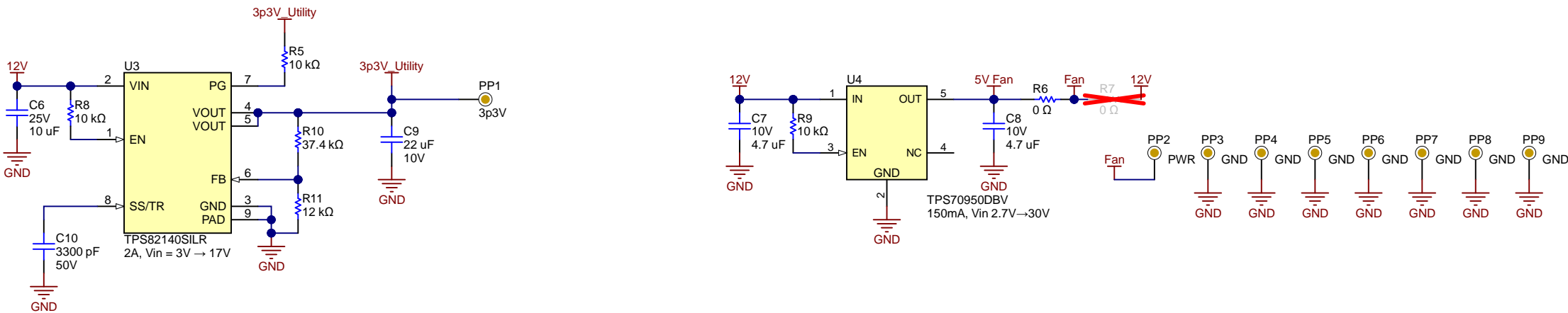
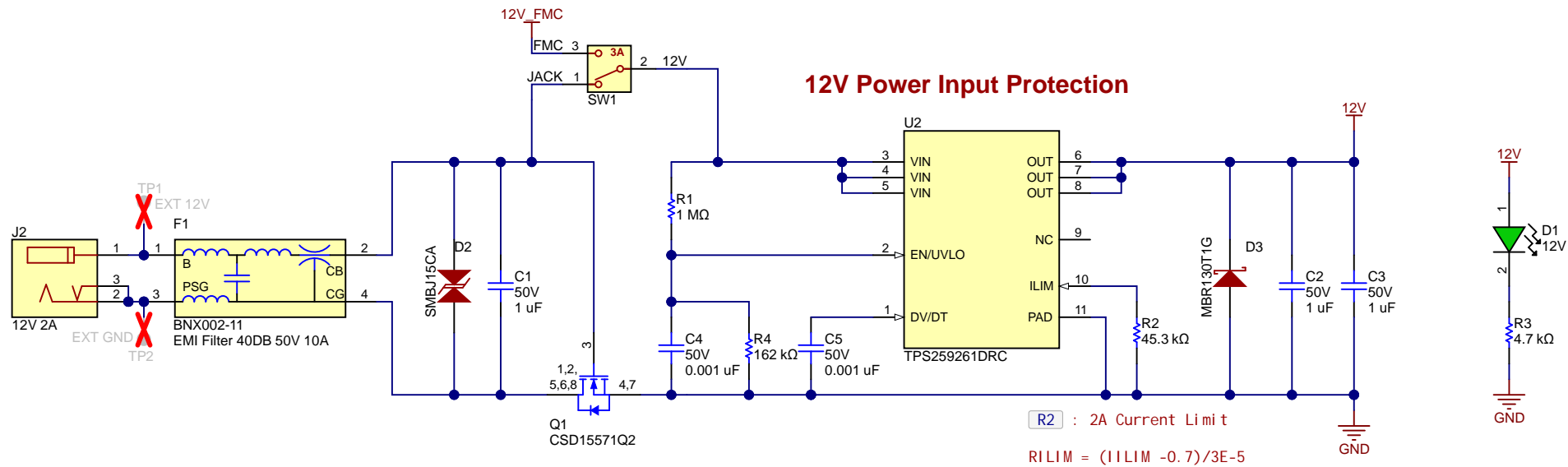
Block Diagram



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Orderable: <a href="#">ChangeMe in variant</a>		Designed for: <a href="#">Public Release</a>	Mod. Date: 8/13/2024
TID #: <a href="#">N/A</a>		Project Title: <a href="#">DAC39RF20EVM</a>	
Number: <a href="#">DC363</a>	Rev: <a href="#">E1</a>	Sheet Title: <a href="#">Block Diagram</a>	
SVN Rev: <a href="#">093cb5ca7a95023ded1b0e51f1074402001</a>		Sheet: <a href="#">1</a> of <a href="#">21</a>	
Drawn By: <a href="#">MK</a>		File: <a href="#">Block Diagram.SchDoc</a>	Size: <a href="#">B</a>
Engineer: <a href="#">MK</a>		Contact: <a href="#">http://www.ti.com/support</a>	

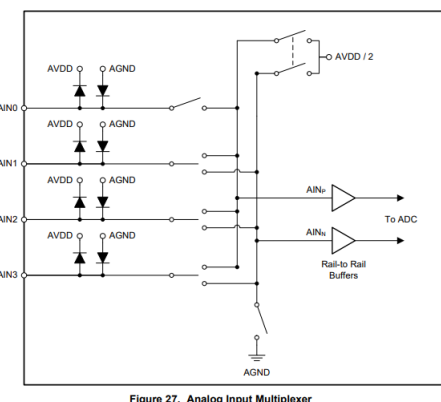
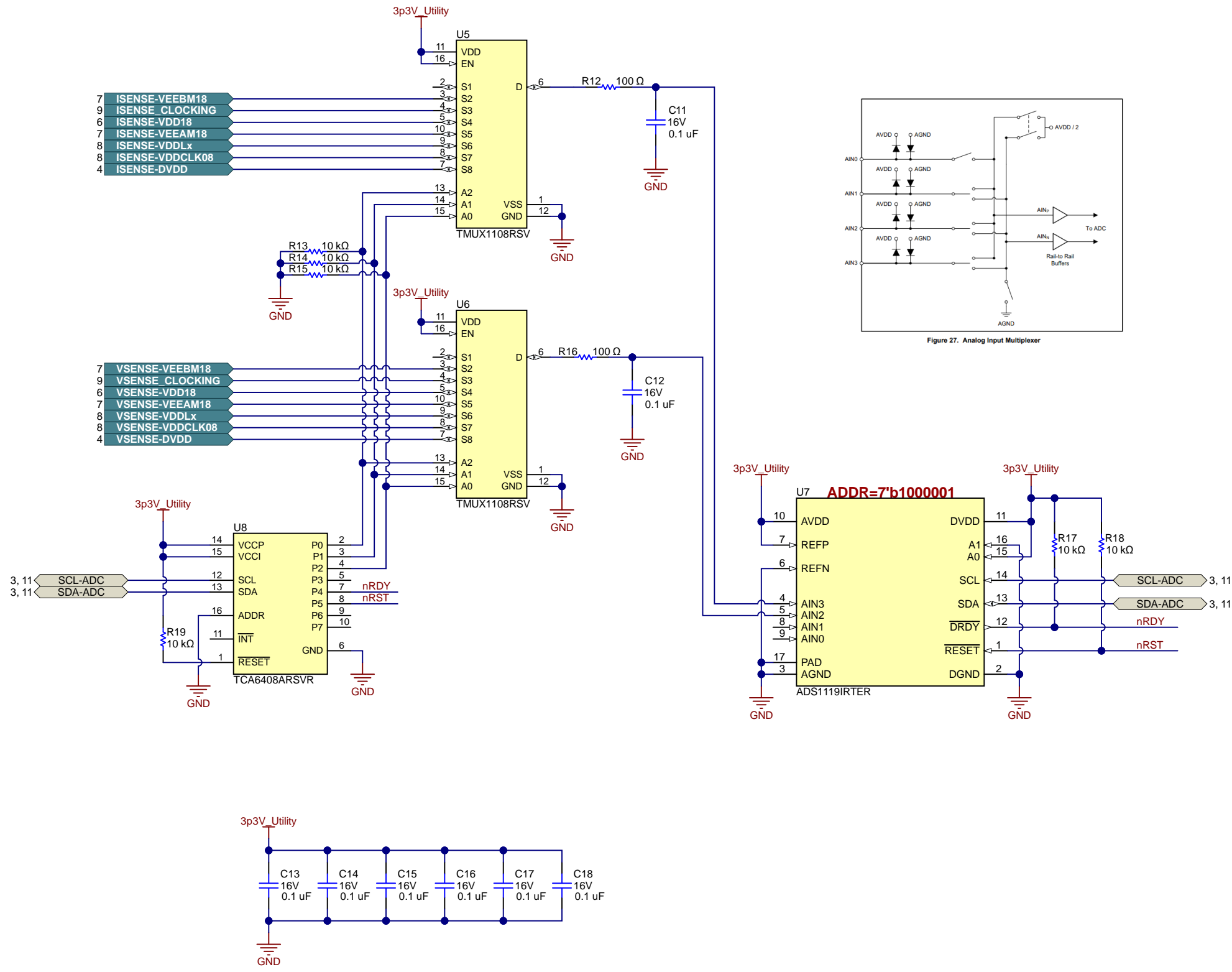
12V Input & 3.3V Utility



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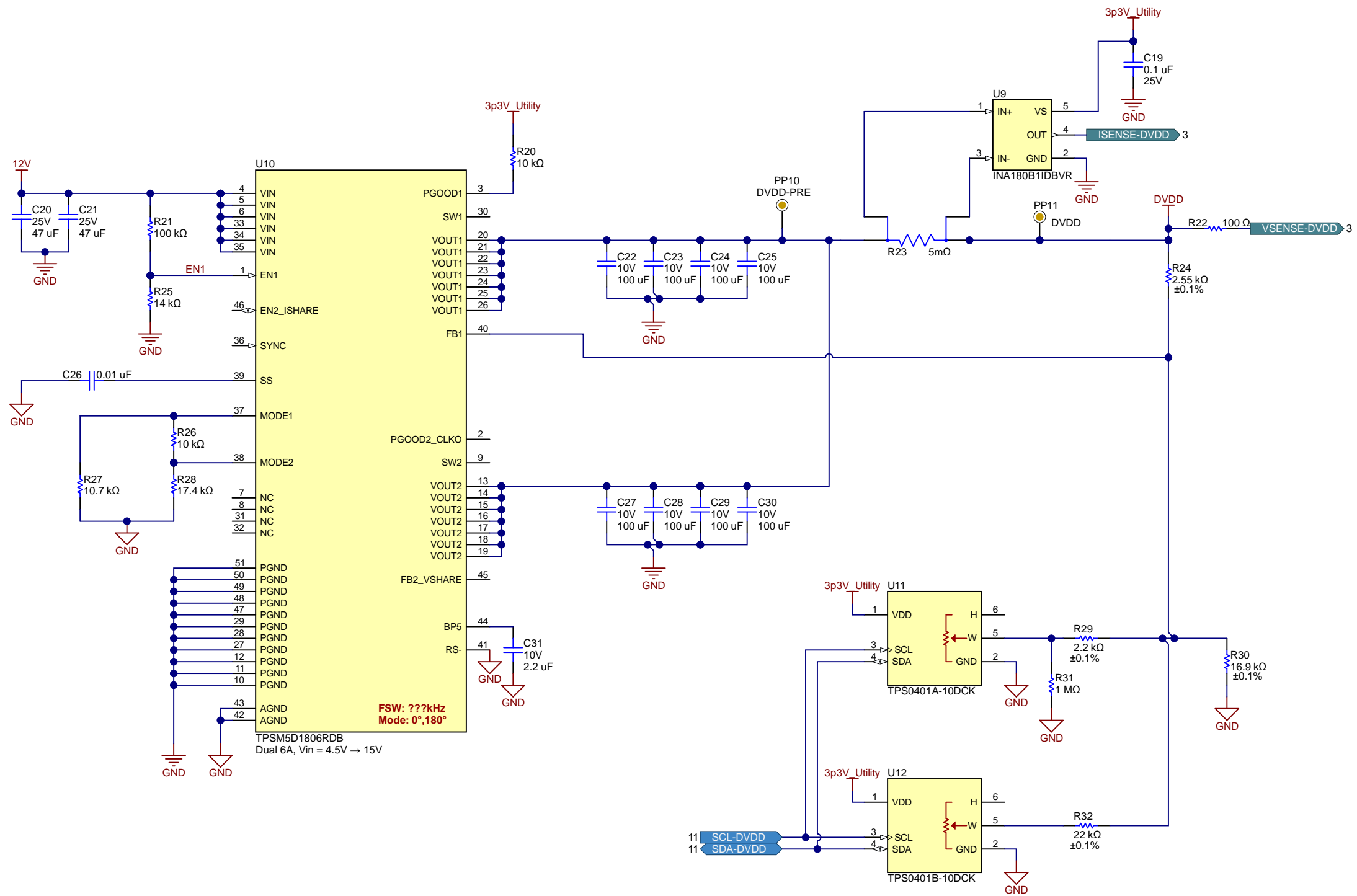
Orderable: <a href="#">ChangeMe in variant</a>	Designed for: <a href="#">Public Release</a>	Mod. Date: 1/24/2025
TID #: <a href="#">N/A</a>	Project Title: <a href="#">DAC39RF20EVM</a>	
Number: <a href="#">DC363</a>	Rev: <a href="#">E1</a>	Sheet Title: <a href="#">12V Input &amp; 3.3V Utility</a>
SVN Rev: <a href="#">e25fa76b6baa0590a0ec0d40b4a09015</a> [Locally Modified]	Sheet: <a href="#">2</a> of <a href="#">21</a>	
Drawn By: <a href="#">MK</a>	File: <a href="#">12V Input, Efuse and 3p3V Utility.SchDoc</a>	Size: <a href="#">B</a>
Engineer: <a href="#">MK</a>	Contact: <a href="#">http://www.ti.com/support</a>	

Sense ADC



ADS1119RTE Addresses		
A0	A1	Addr
GND	GND	0x40
GND	DVDD	0x41
GND	SDA	0x42
GND	SCL	0x43
DVDD	GND	0x44
DVDD	DVDD	0x45
DVDD	SDA	0x46
DVDD	SCL	0x47
SDA	GND	0x48
SDA	DVDD	0x49
SDA	SDA	0x4A
SDA	SCL	0x4B
SCL	GND	0x4C
SCL	DVDD	0x4D
SCL	SDA	0x4E
SCL	SCL	0x4F

DAC DVDD Rail



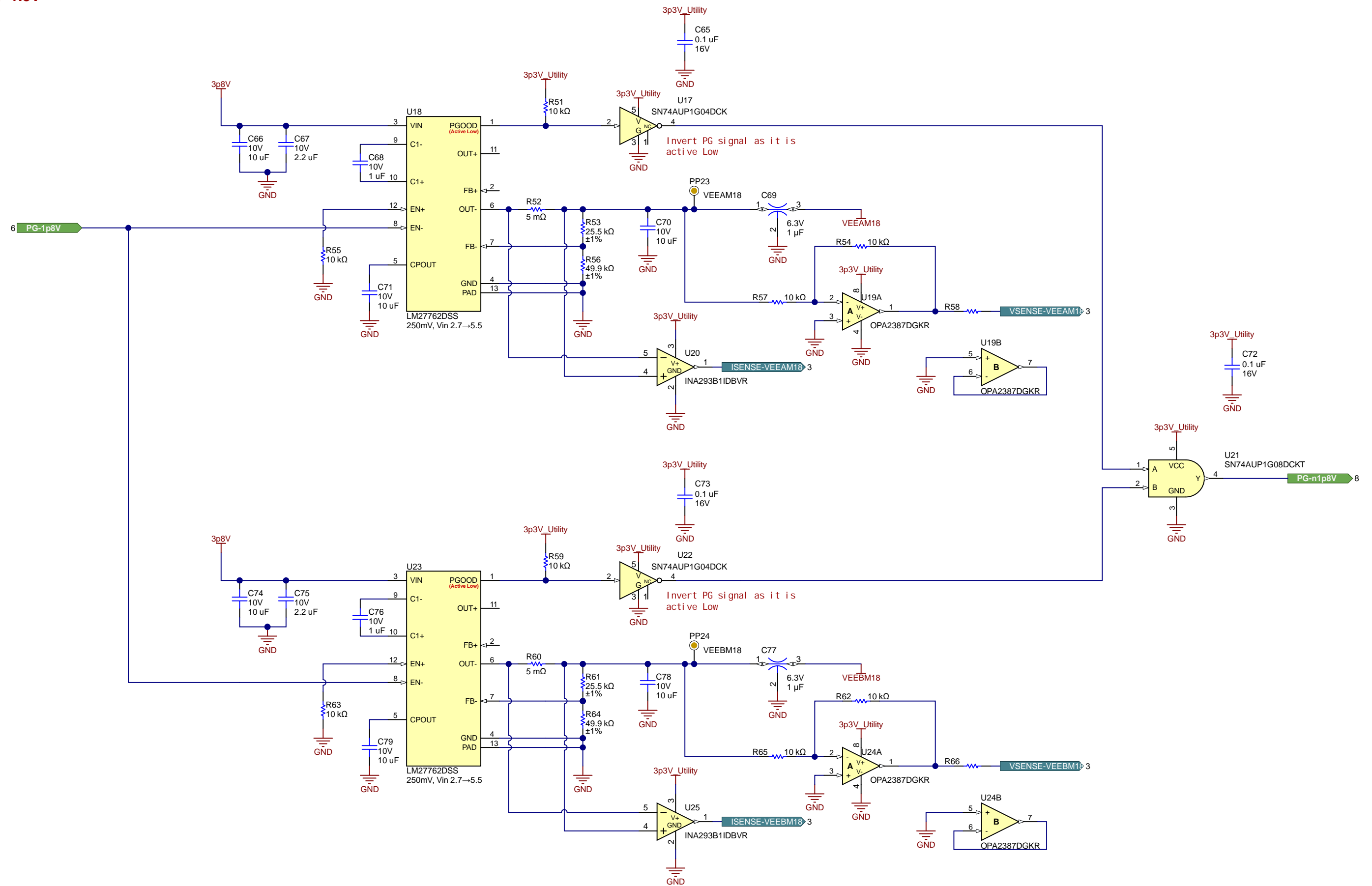
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TID #: <a href="#">N/A</a>	Project Title: <a href="#">DAC39RF20EVM</a>	
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SVN Rev: <a href="#">e25fa76b6baa0590a0ec0d4c1b4081a09075</a> [Locally Modified]	Sheet: <a href="#">4</a> of <a href="#">21</a>	
Drawn By: <a href="#">MK</a>	File: <a href="#">Power DC-DC Digital.SchDoc</a>	Size: <a href="#">B</a>
Engineer: <a href="#">MK</a>	Contact: <a href="#">http://www.ti.com/support</a>	





## DAC Analog -1.8V



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TID #: <a href="#">N/A</a>	Project Title: <a href="#">DAC39RF20EVM</a>		
Number: <a href="#">DC93</a>	Rev: <a href="#">E1</a>	Sheet Title: <a href="#">DAC Analog-1.8V</a>	
SVN Rev: <a href="#">e25fa76b6baa0590a0ec0d444b10544009a075</a> [Locally Modified]		Sheet: <a href="#">7</a> of <a href="#">21</a>	
Drawn By:	File: <a href="#">Power LDO N1p8V Analog.SchDoc</a>	Size: B	
Engineer: <a href="#">MK</a>	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>		

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DAC Analog 0.8V & 1V

A

B

C

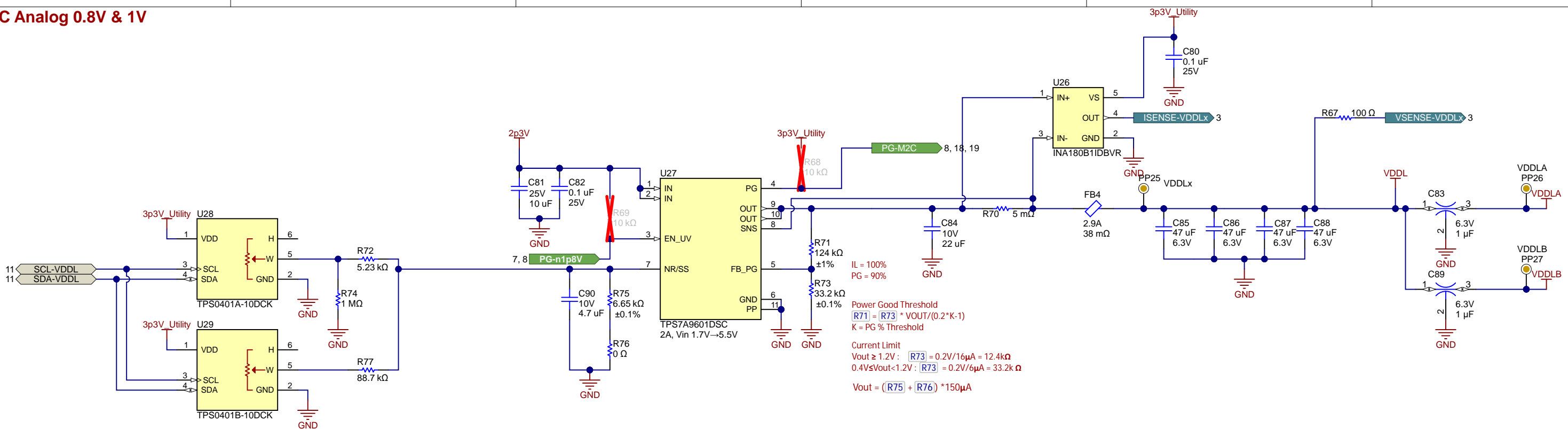
D

A

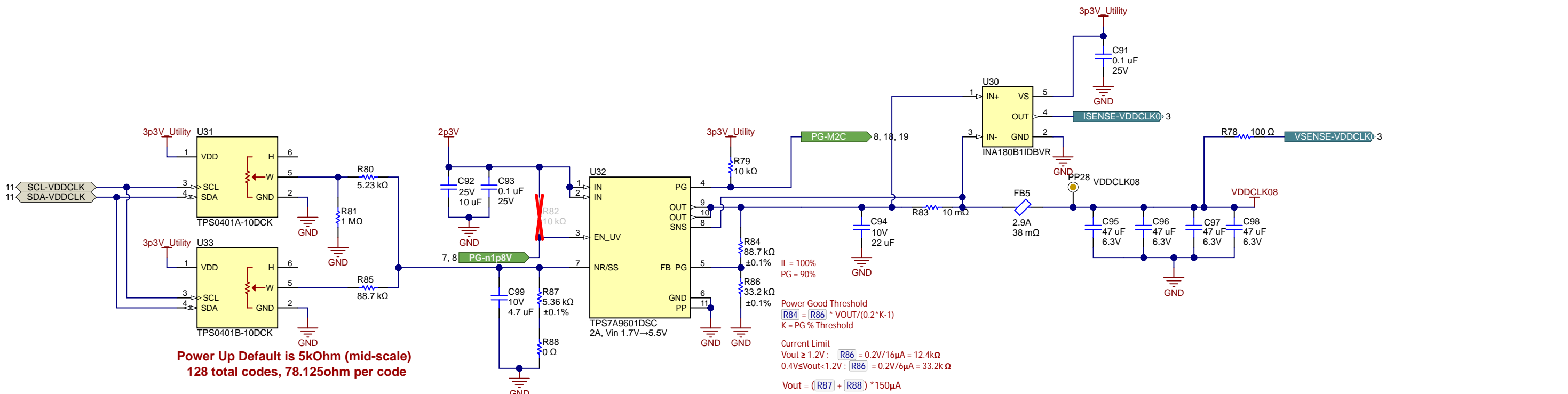
B

C

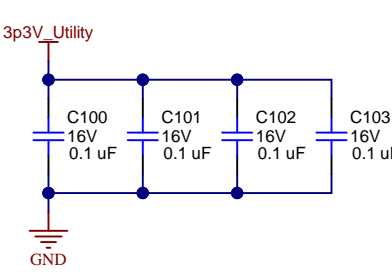
D



Power Up Default is 5kOhm (mid-scale)  
128 total codes, 78.125ohm per code



Power Up Default is 5kOhm (mid-scale)  
128 total codes, 78.125ohm per code



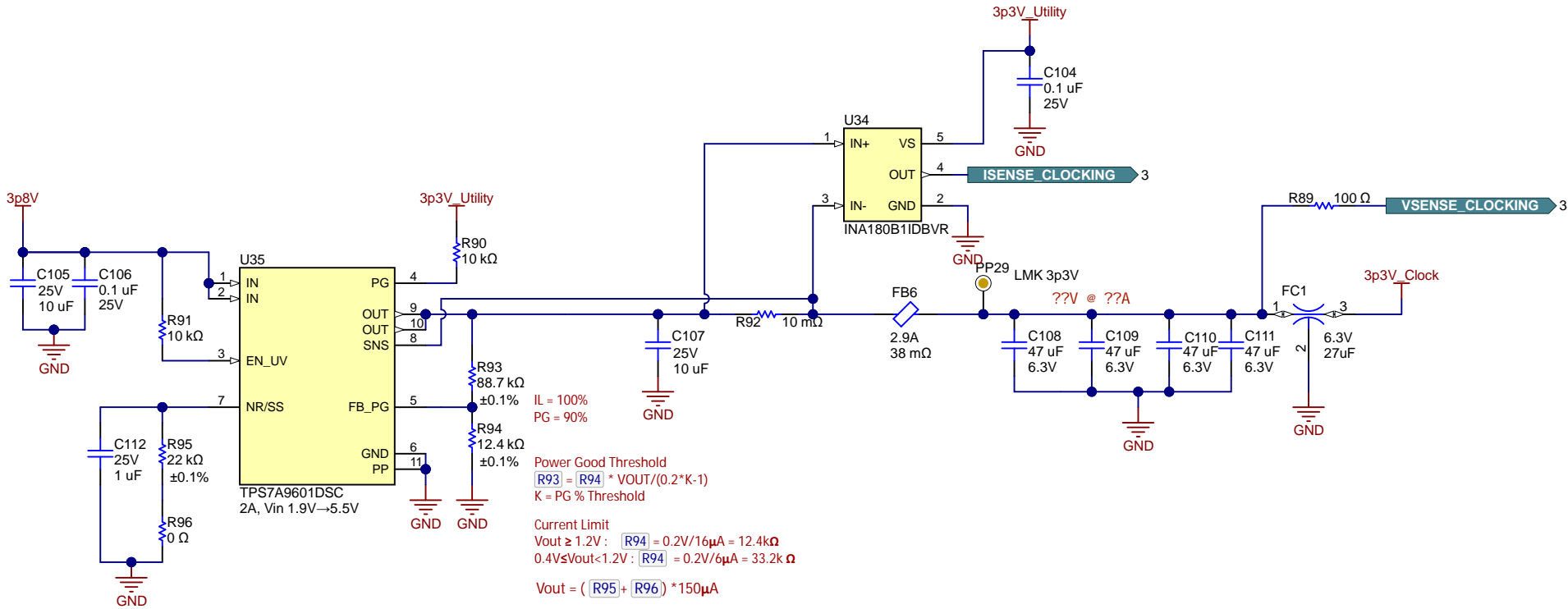
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Orderable: <a href="#">ChangeMe in variant</a>	Designed for: Public Release	Mod. Date: 1/24/2025
TID #: N/A	Project Title: DAC39RF20EVM	
Number: DC363	Rev: E1	Sheet Title: DAC Analog 0.8V & 1V
SVN Rev: e25fa76b6baa0590a0ec0d40b4084a09075 [Locally Modified]	Added: 1/24/2025	Sheet: 8 of 21
Drawn By:	File: Power LDO 0p8V Analog.SchDoc	Size: B
Engineer: MK	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	





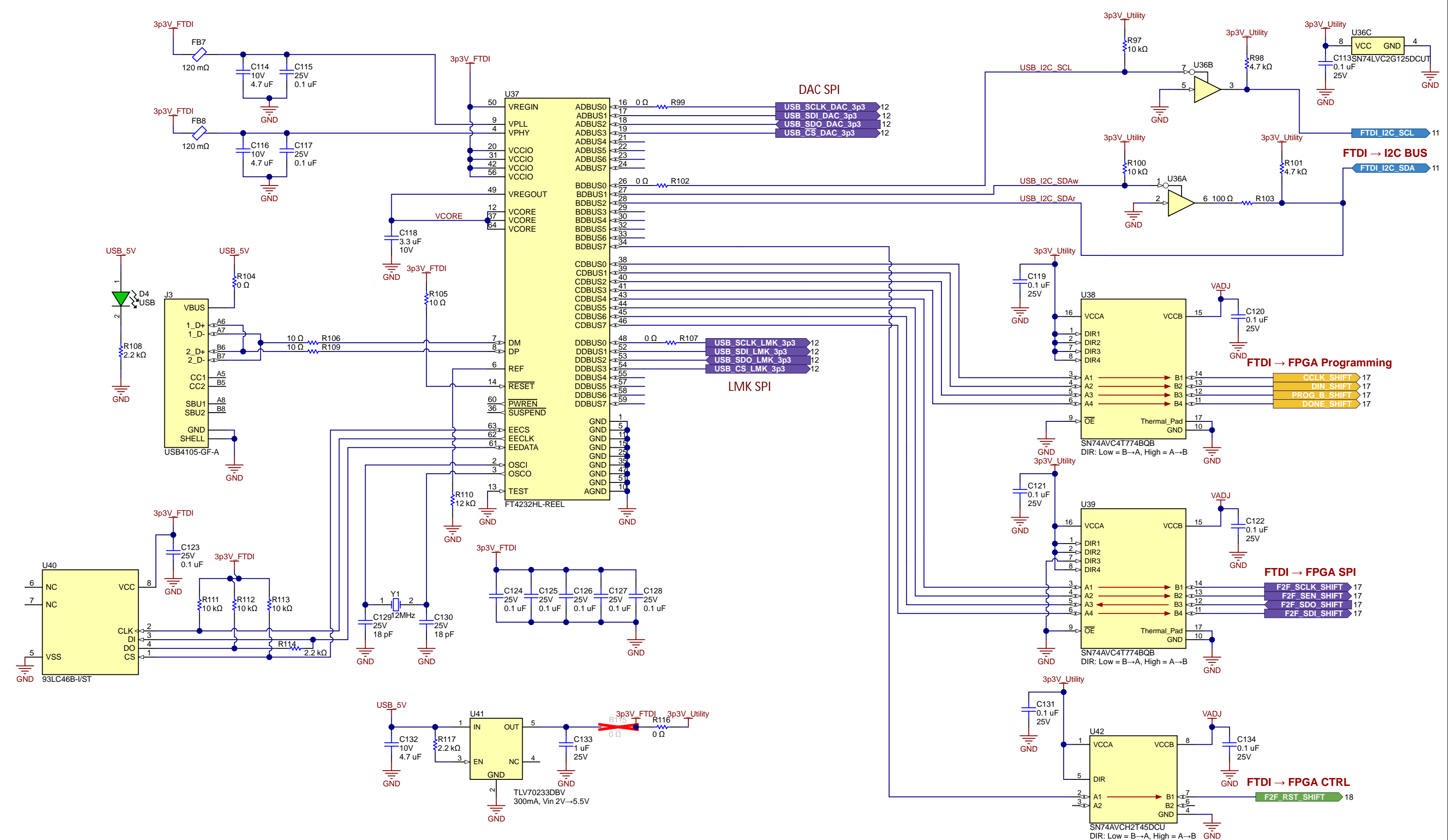
LMK 3.3V Power



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TID #: <a href="#">N/A</a>	Project Title: <a href="#">DAC39RF20EVM</a>	
Number: <a href="#">DC363</a>	Rev: <a href="#">E1</a>	Sheet Title: <a href="#">LMK 3.3V Power</a>
SVN Rev: <a href="#">e25fa76b6baa0590a0ec0d40840090015</a> [Locally Modified]	Sheet: <a href="#">9</a> of <a href="#">21</a>	
Drawn By: <a href="#">MK</a>	File: <a href="#">Power LMK.SchDoc</a>	Size: <a href="#">B</a>
Engineer: <a href="#">MK</a>	Contact: <a href="#">http://www.ti.com/support</a>	

## FTDI Control

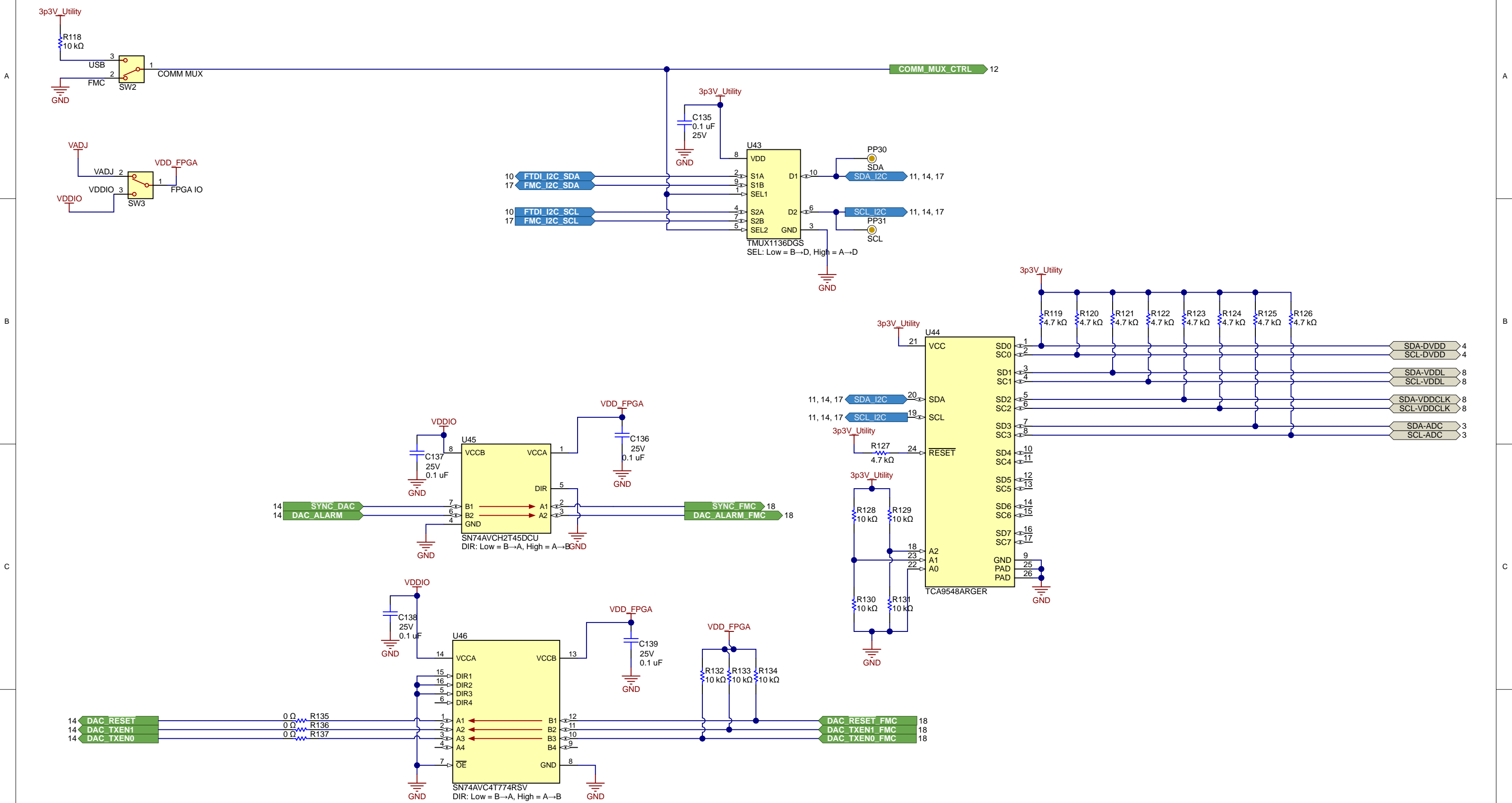


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TID #: <a href="#">N/A</a>	Project Title: <a href="#">DAC39RF20EVM</a>	
Number: <a href="#">DC363</a>	Rev: <a href="#">E1</a>	Sheet Title: <a href="#">FTDI Control</a>
SVN Rev: <a href="#">e25fa76bbaa0590a0ec044440b34d09a075</a> [Locally Modified]		Sheet: 10 of 21
Drawn By:	File: <a href="#">USB Control FTDI.SchDoc</a>	Size: B
Engineer: <a href="#">MK</a>	Contact: <a href="#">http://www.ti.com/support</a>	

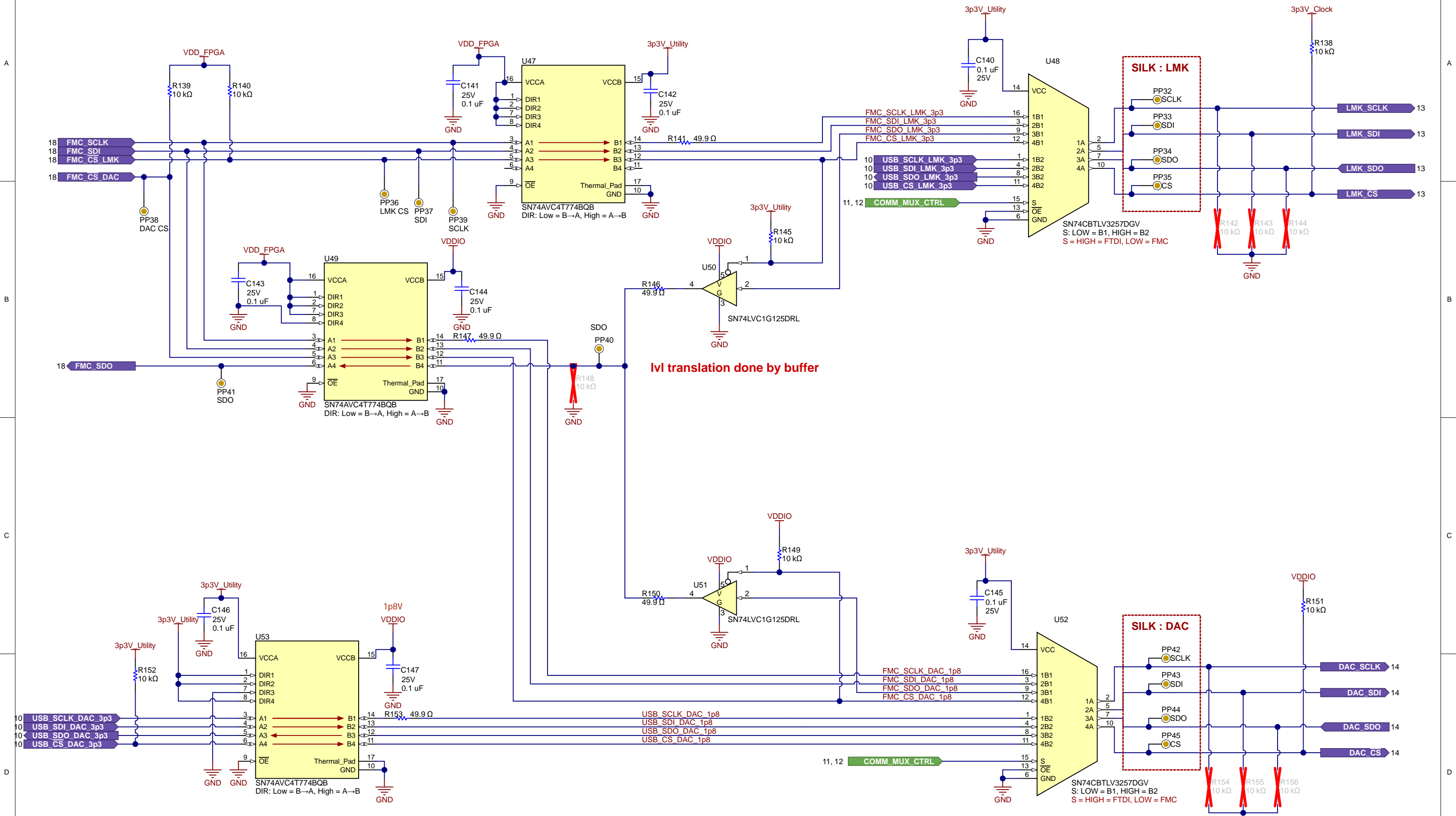


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Comms Lvl Shift & Mux



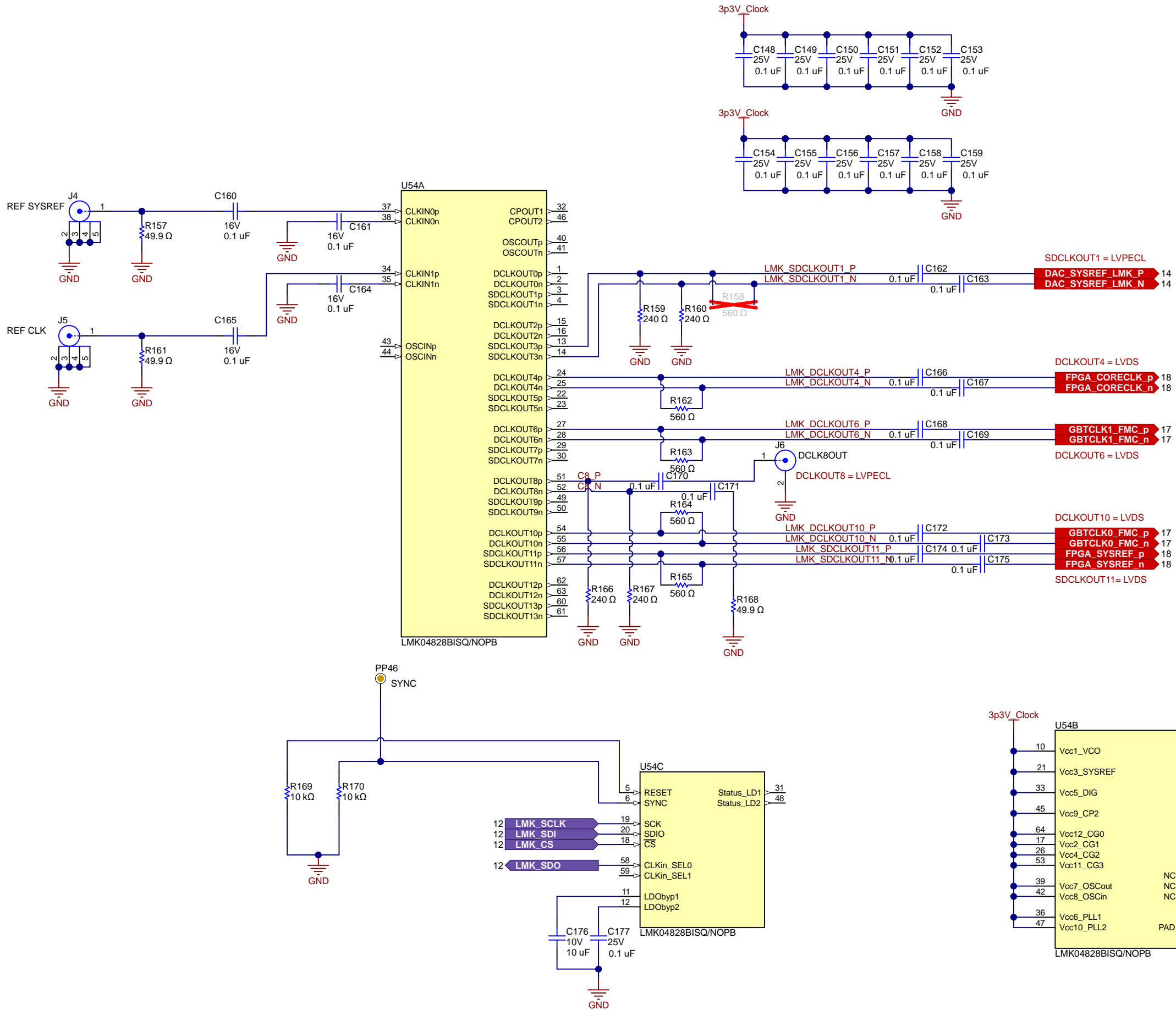
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TID #: <a href="#">N/A</a>	Project Title: <a href="#">DAC39RF20EVM_GND</a>	
Number: <a href="#">DC363</a>	Rev: <a href="#">E1</a>	Sheet Title: <a href="#">&lt;Update Title in Parameters&gt;</a>
SVN Rev: <a href="#">e25fa76b6baa0590a0ec0d40b84009075</a> (Locally Modified)	Sheet: 12 of 21	
Drawn By: <a href="#">MK</a>	File: <a href="#">LMK LVL Shift and Mux.SchDoc</a>	Size: B
Engineer: <a href="#">MK</a>	Contact: <a href="#">http://www.ti.com/support</a>	

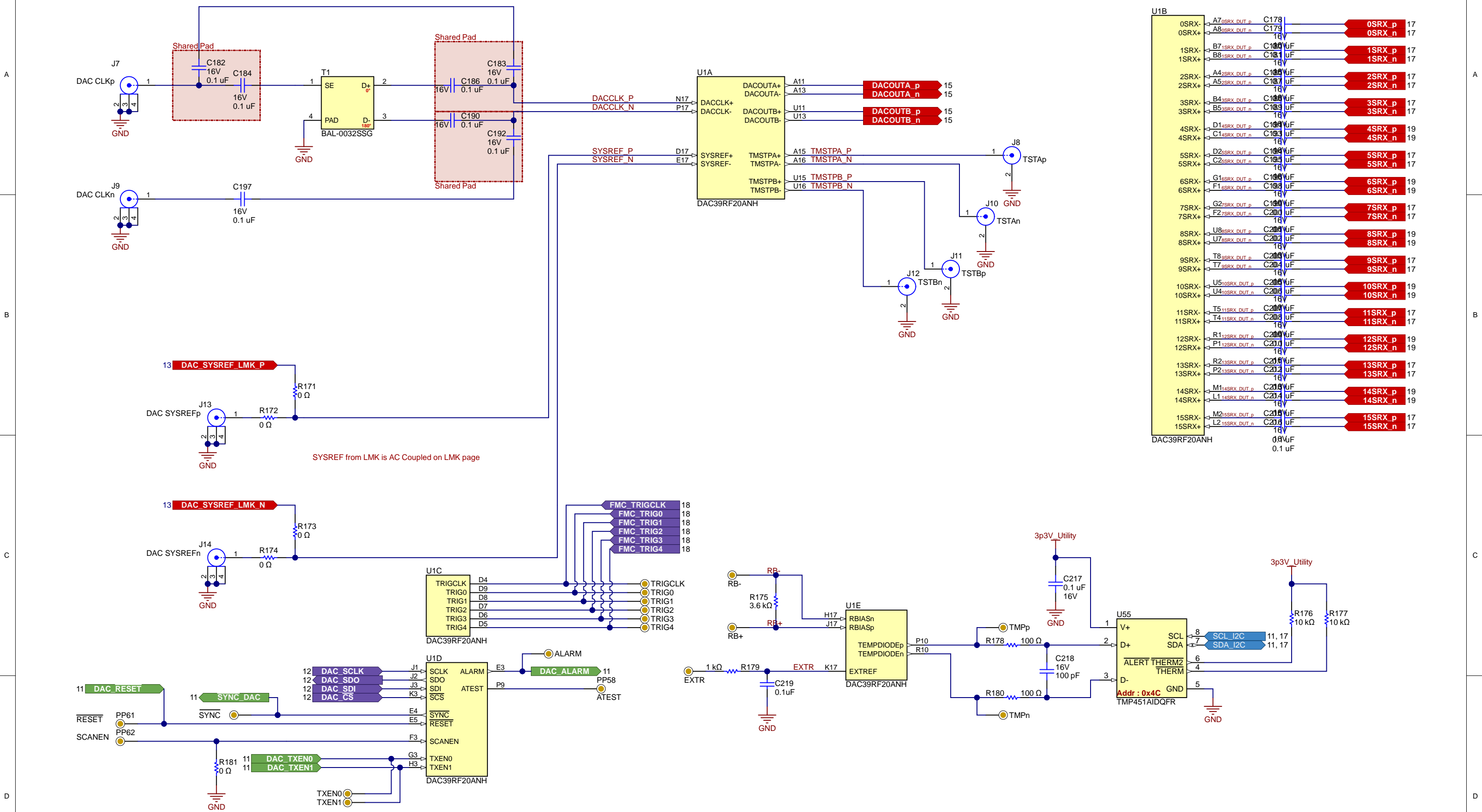
LMK Clocking Fanout



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Orderable: <a href="#">ChangeMe</a> in variant	Designed for: <a href="#">Public Release</a>	Mod. Date: 1/24/2025
TID #: <a href="#">N/A</a>	Project Title: <a href="#">DAC39RF20EVM</a>	
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SVN Rev: <a href="#">e25fa76b6baa0590a0ec0d4d40b4a09075</a> [Locally Modified]	Sheet: <a href="#">13</a> of <a href="#">21</a>	
Drawn By: <a href="#">e25fa76b6baa0590a0ec0d4d40b4a09075</a>	File: <a href="#">Clocking LMK04828.SchDoc</a>	Size: <a href="#">B</a>
Engineer: <a href="#">MK</a>	Contact: <a href="#">http://www.ti.com/support</a>	

DAC I/O





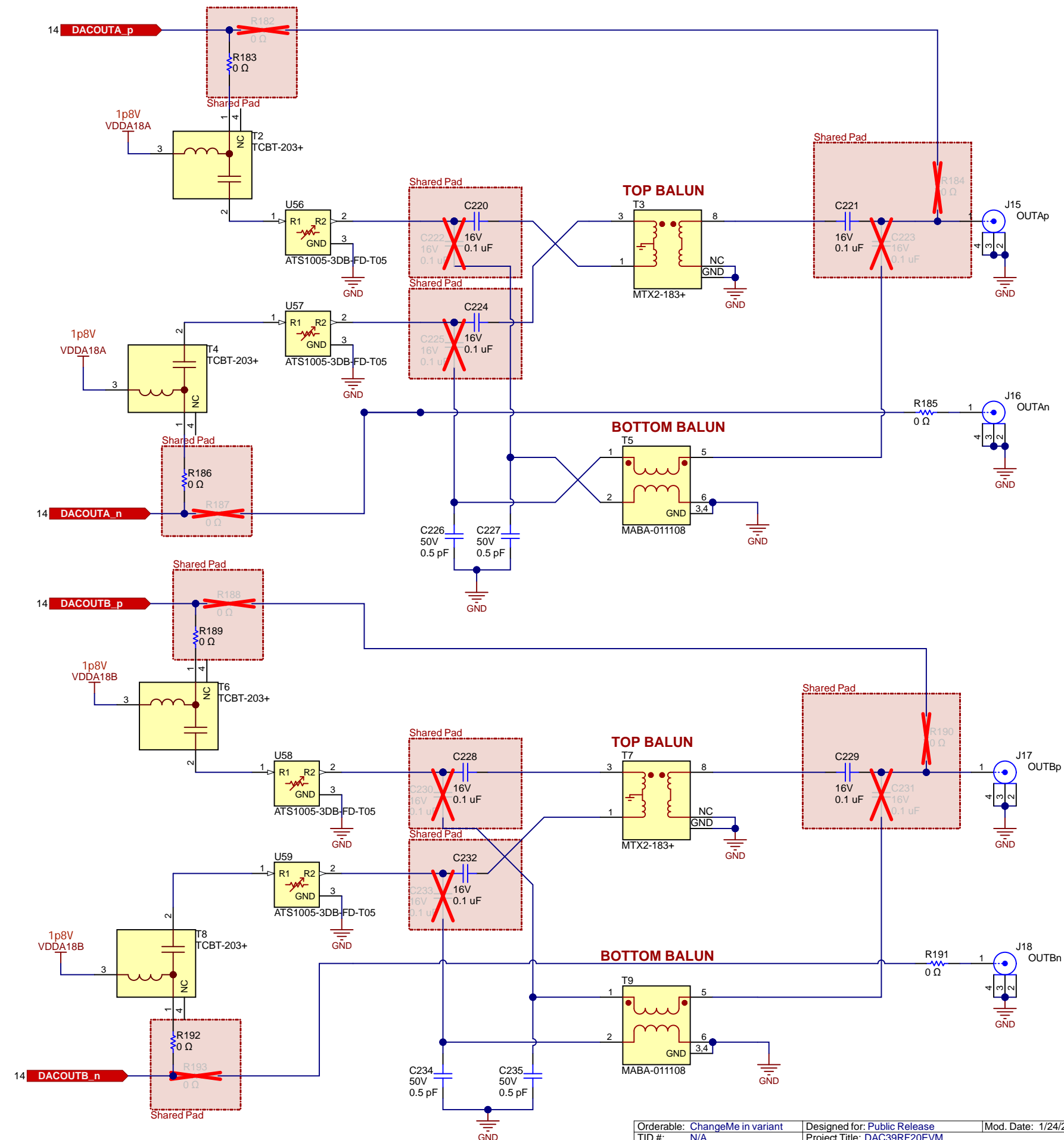
## DAC Outputs

Channel	Balun	Uninstall	Install
A	TCM2-63WX+	Not found Not found	Not found Not found
A	MTX2-183+	Not found Not found	Not found Not found
A	Bypass	Not found Not found	Not found Not found
B	TCM2-63WX+	Not found Not found	Not found Not found
B	MTX2-183+	Not found Not found	Not found Not found
B	Bypass	Not found Not found	Not found Not found

### DACA default to lower band balun TCM2-63WX+ (1st Nyquist)

## DACA 180° Phase for layout

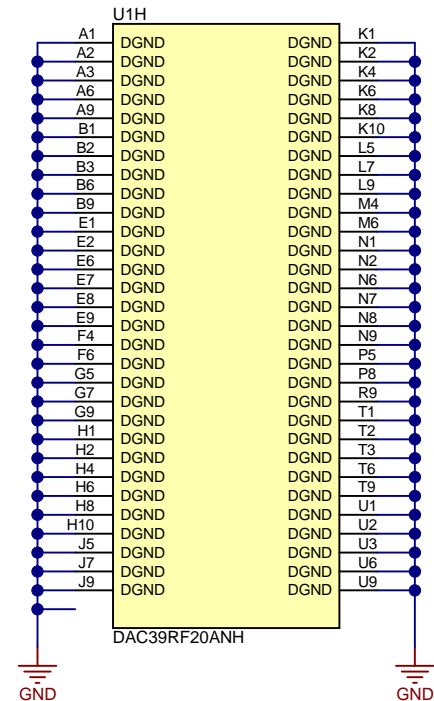
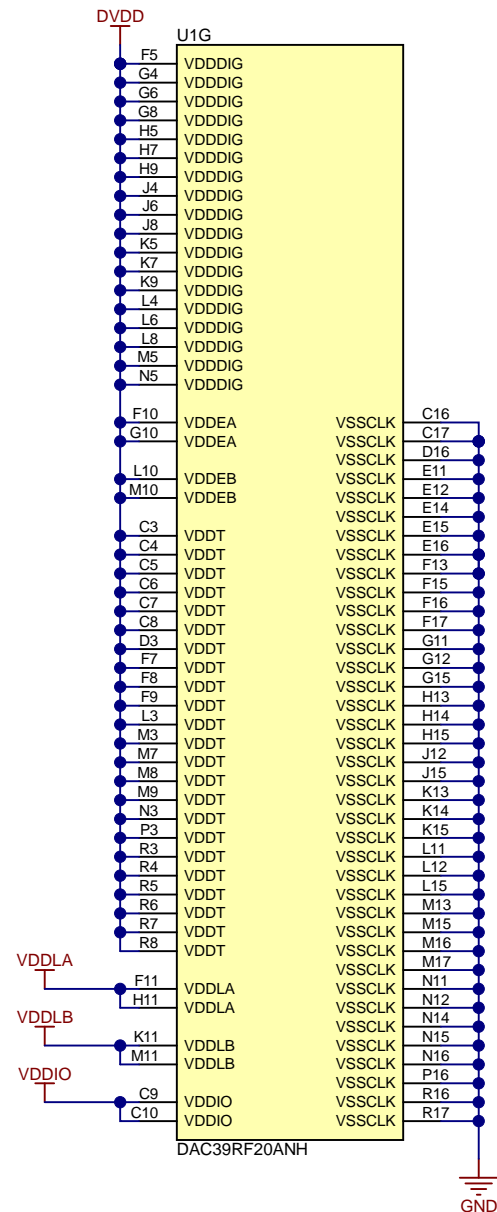
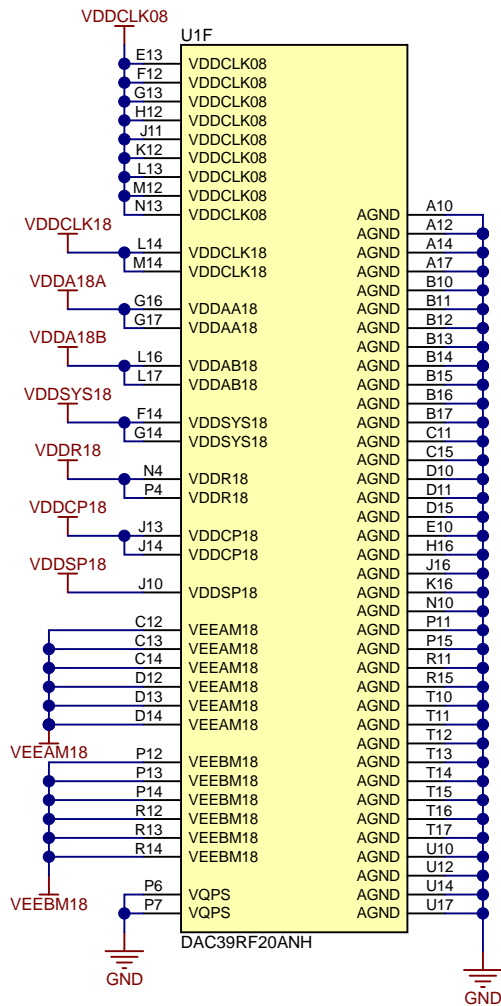
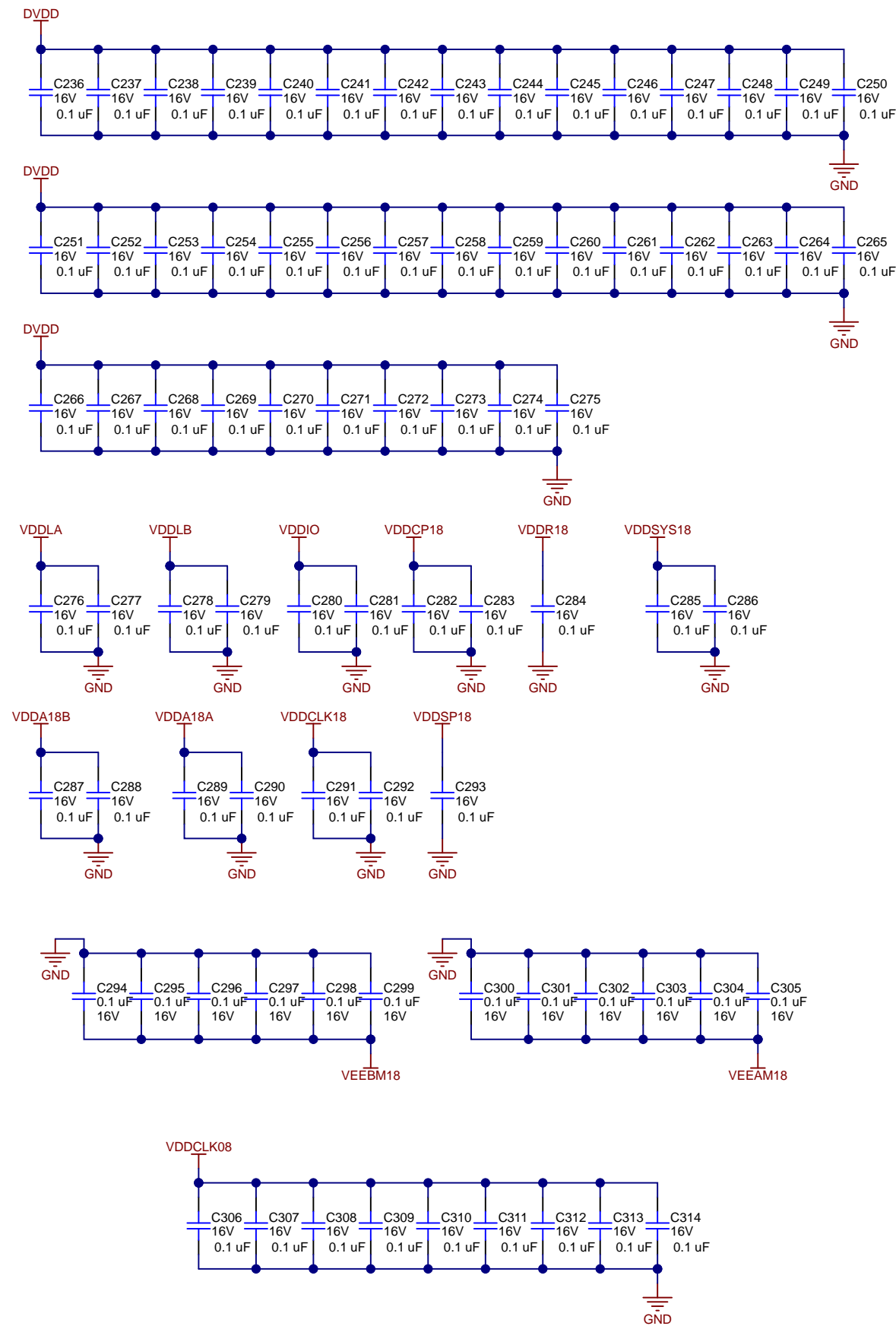
**DACB default to higher band MMIC balun MTX2-183+ (multi-Nyquist)**



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Orderable: <a href="#">ChangeMe in variant</a>	Designed for: <a href="#">Public Release</a>	Mod. Date: 1/24/2025
TID #: <a href="#">N/A</a>	Project Title: <a href="#">DAC39RF20EVM</a>	
Number: <a href="#">DC363</a>	Rev: <a href="#">E1</a>	Sheet Title: <a href="#">DAC Outputs</a>
SVN Rev: <a href="#">e25fa76b6aa0590a0ec04404784109075</a> [Locally Modified]		Sheet: <a href="#">15</a> of <a href="#">21</a>
Drawn By:	File: <a href="#">DUT Outputs.SchDoc</a>	Size: B
Engineer: <a href="#">MK</a>	Contact: <a href="#">http://www.ti.com/support</a>	

## DAC39RF20 Power Connections





FMC+ Section Rows A - E

A

B

C

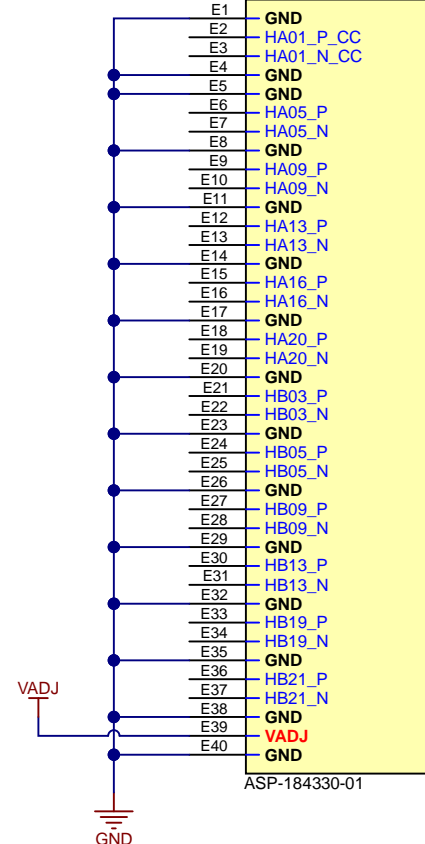
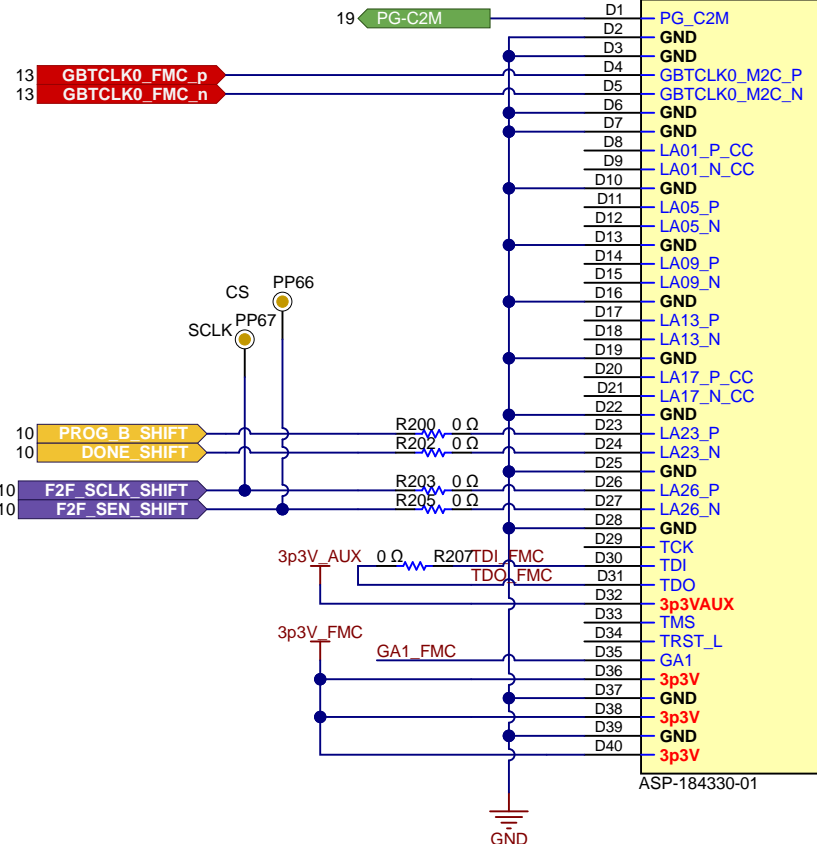
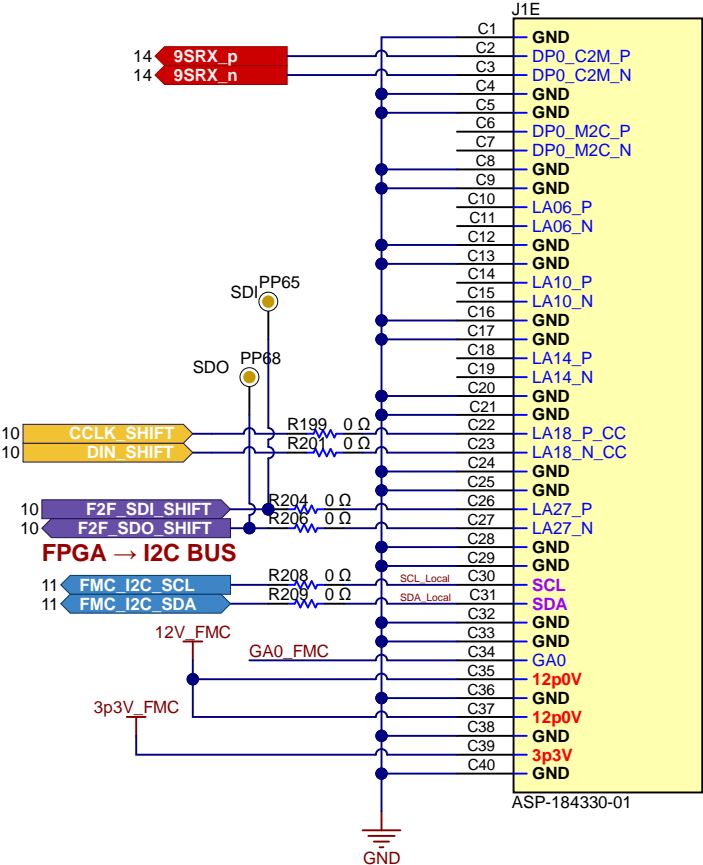
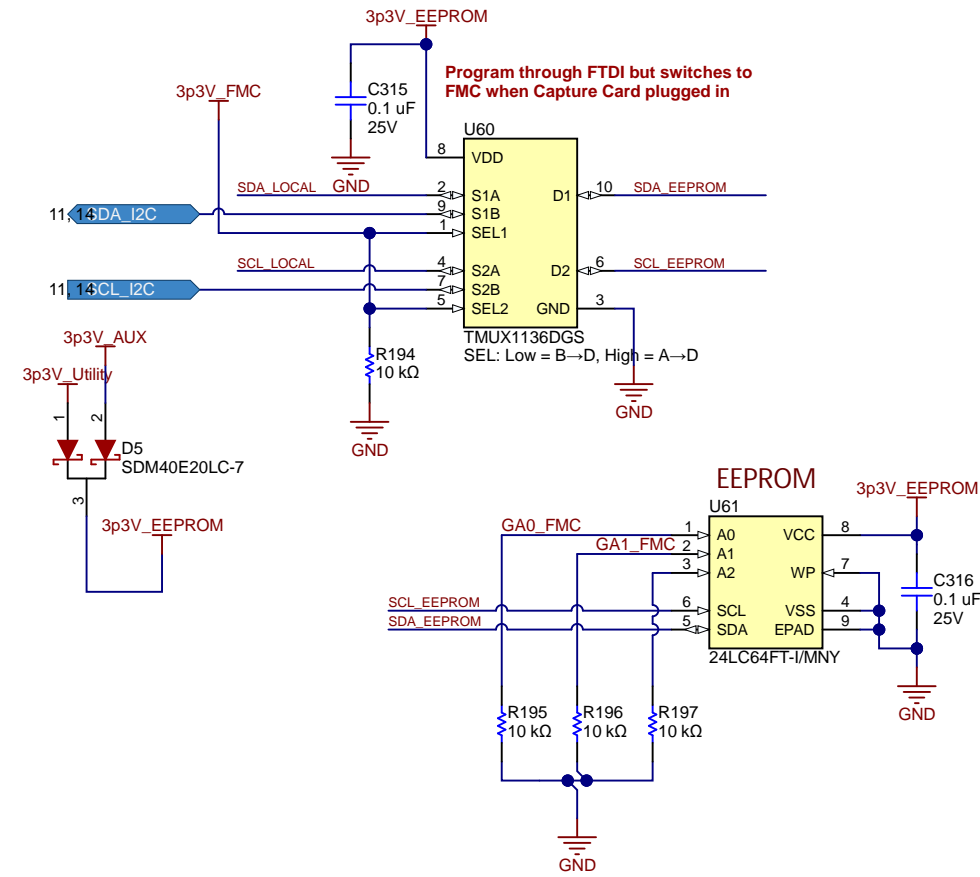
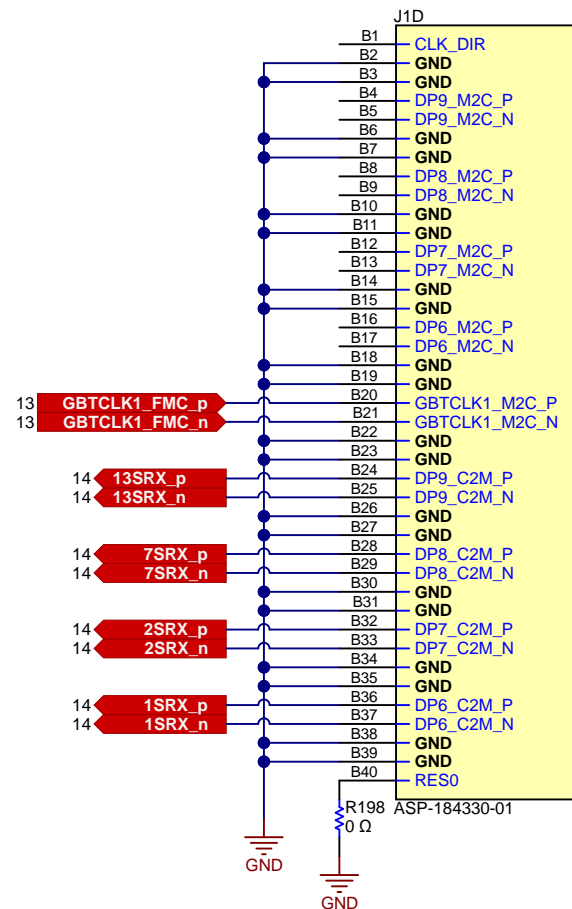
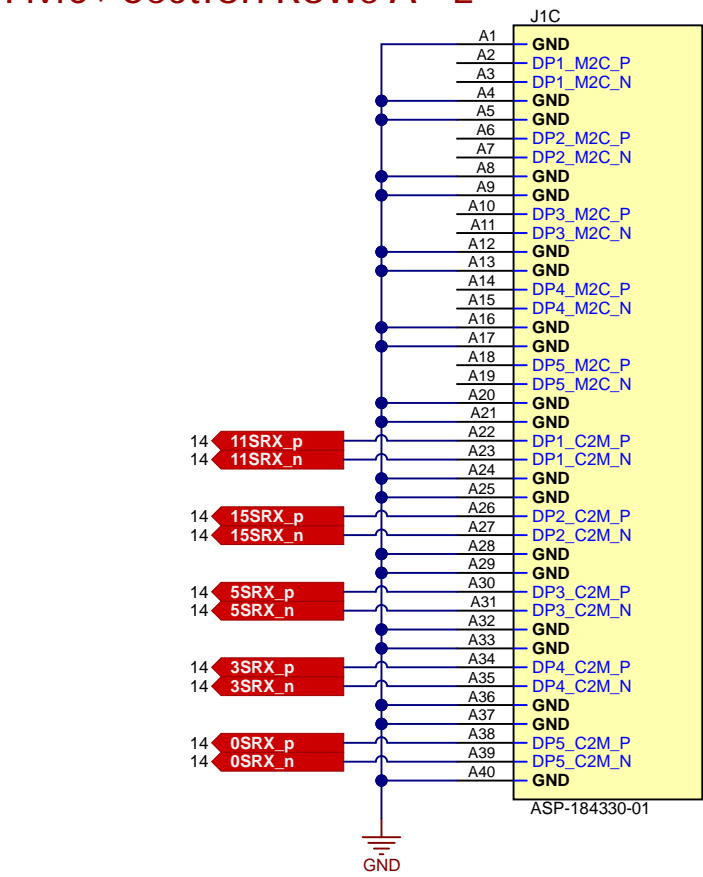
D

A

B

C

D



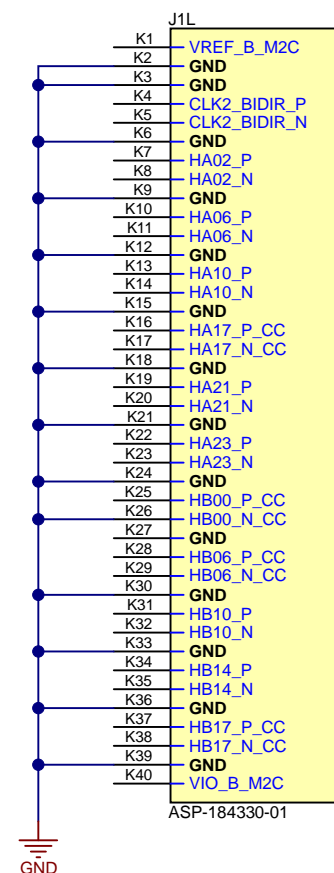
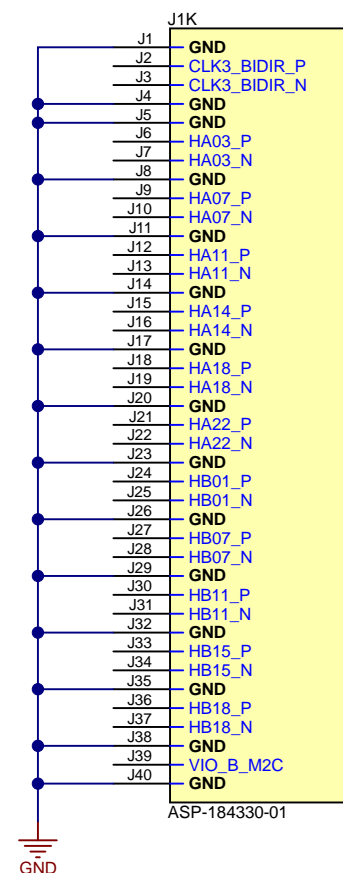
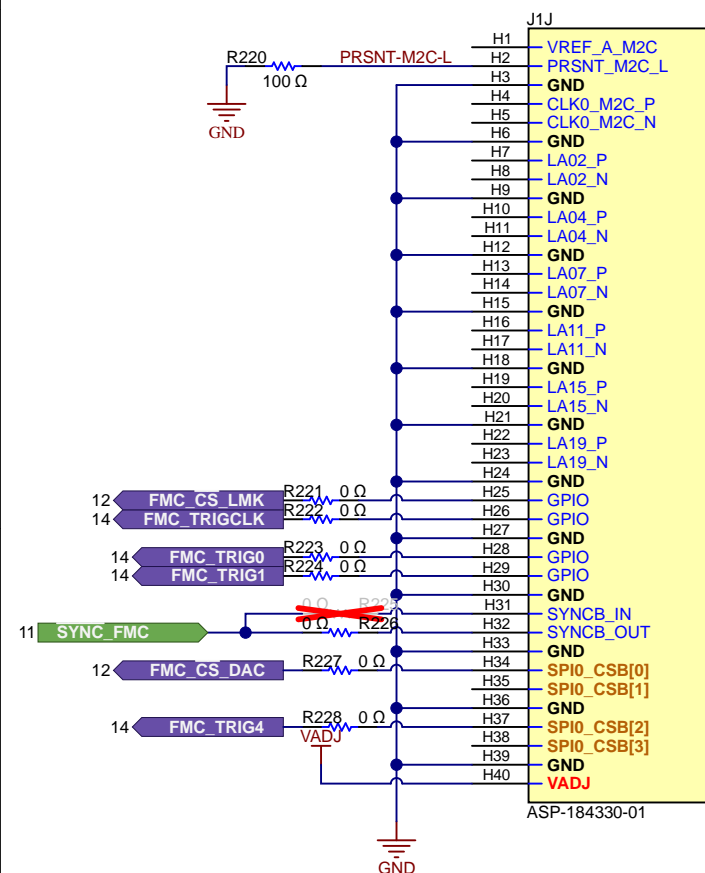
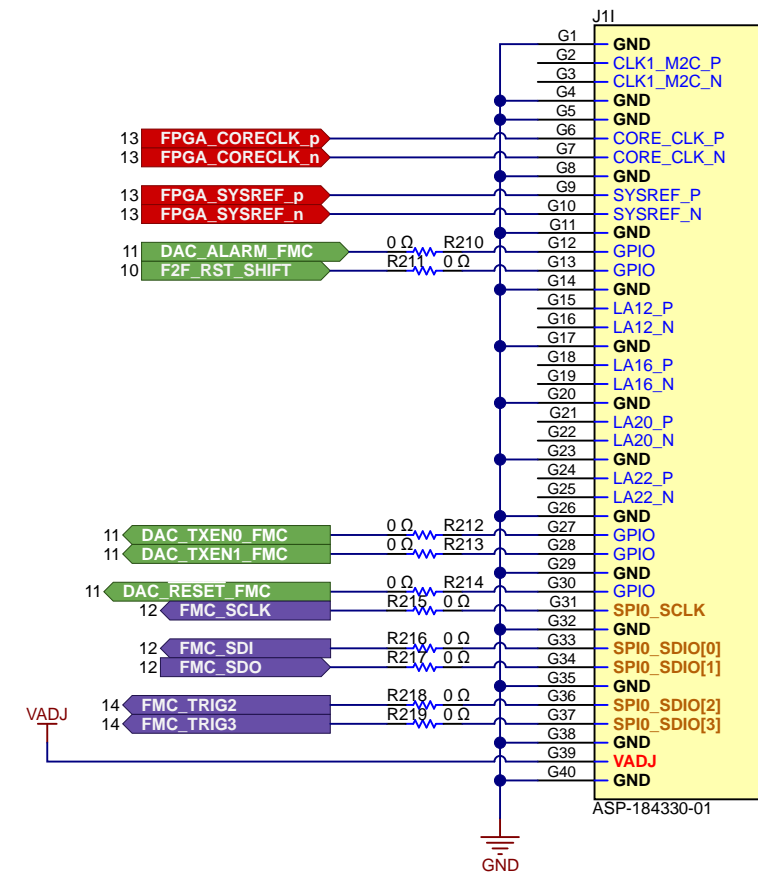
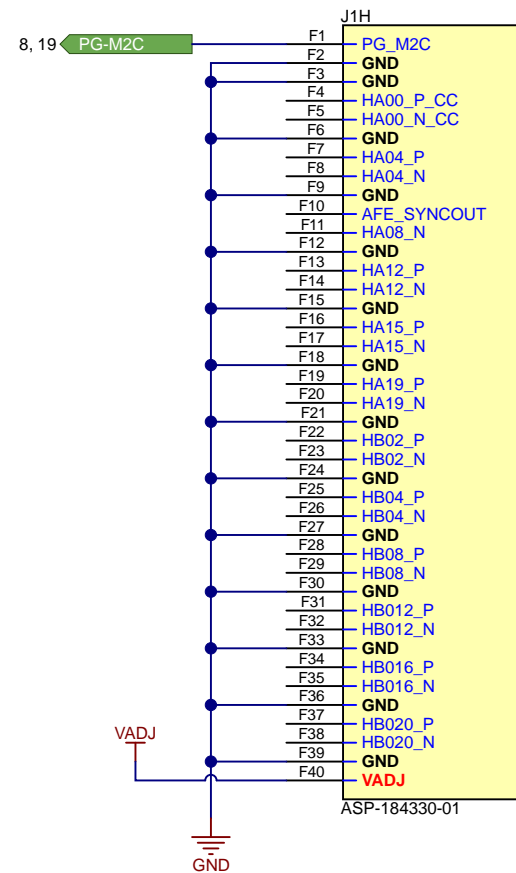
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TID #: <a href="#">N/A</a>	Project Title: <a href="#">DAC39RF20EVM</a>	
Number: <a href="#">DC363</a>	Rev: <a href="#">E1</a>	Sheet Title: <a href="#">FMC+ Section Rows A - E</a>
SVN Rev: <a href="#">e25fa76b6baa0590a0ec0d4010684009075</a> [Locally Modified]	Sheet: <a href="#">17 of 21</a>	
Drawn By: <a href="#">Adarsh V B</a>	File: <a href="#">FMC+ Sections A-E.SchDoc</a>	Size: <a href="#">B</a>
Engineer: <a href="#">MK</a>	Contact: <a href="#">http://www.ti.com/support</a>	

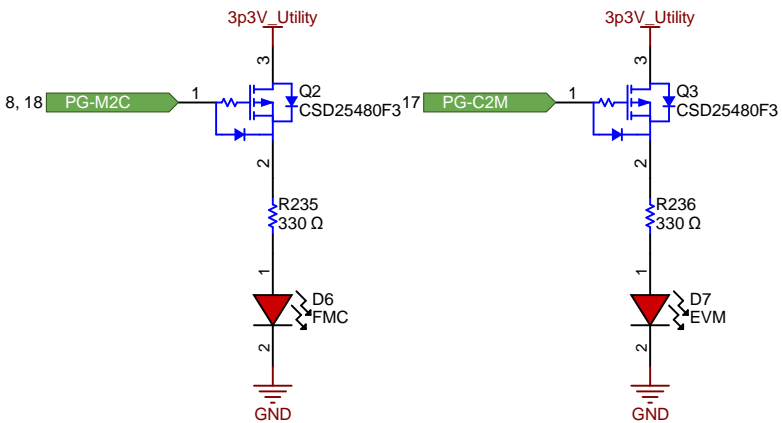
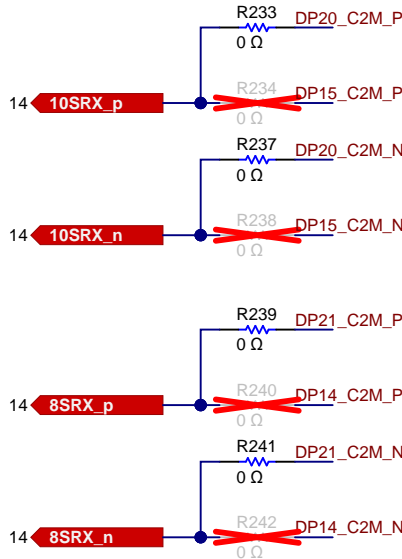
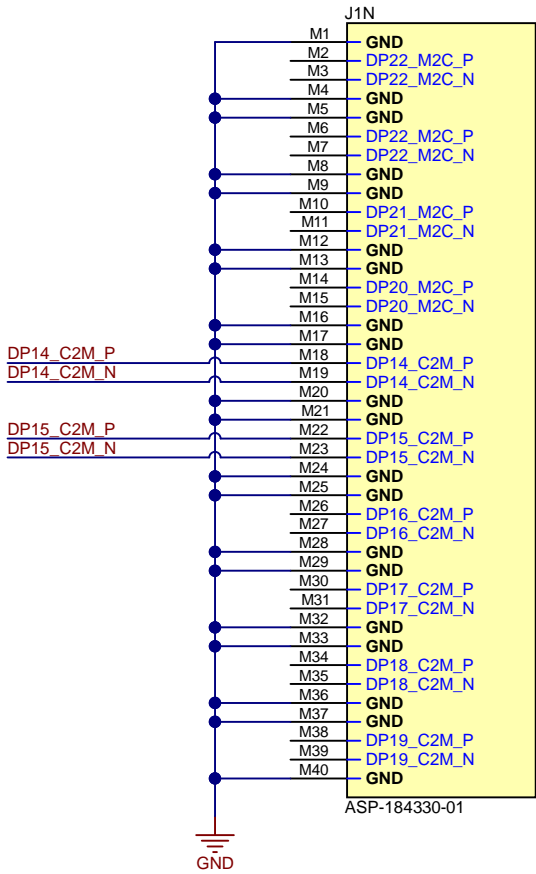
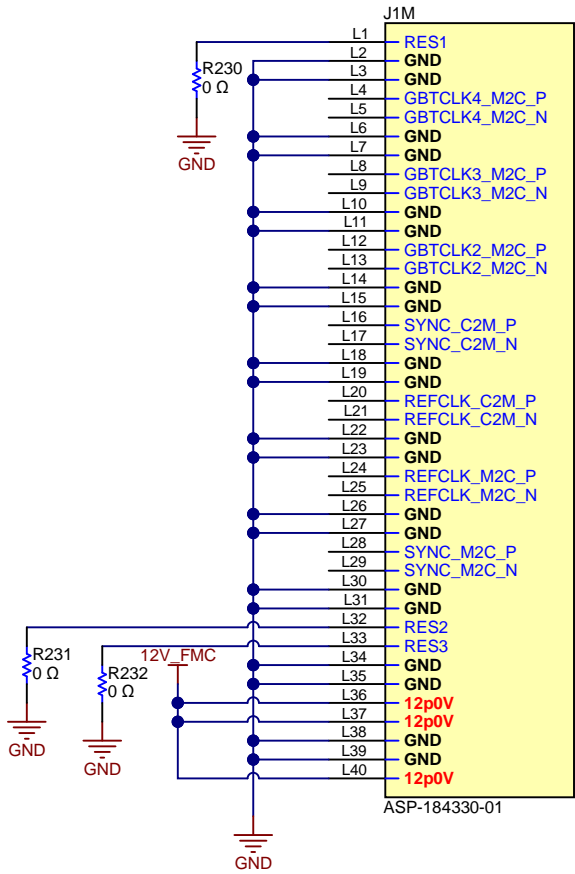
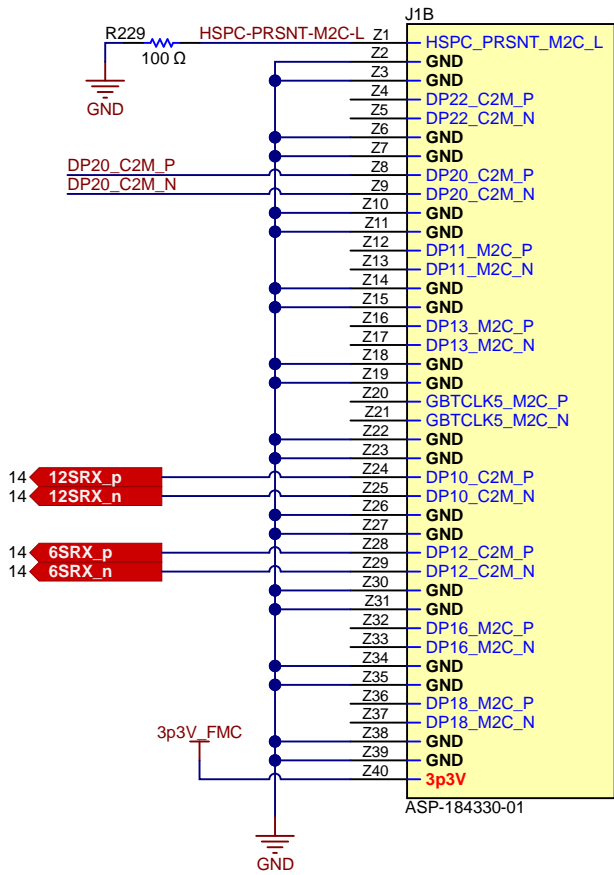
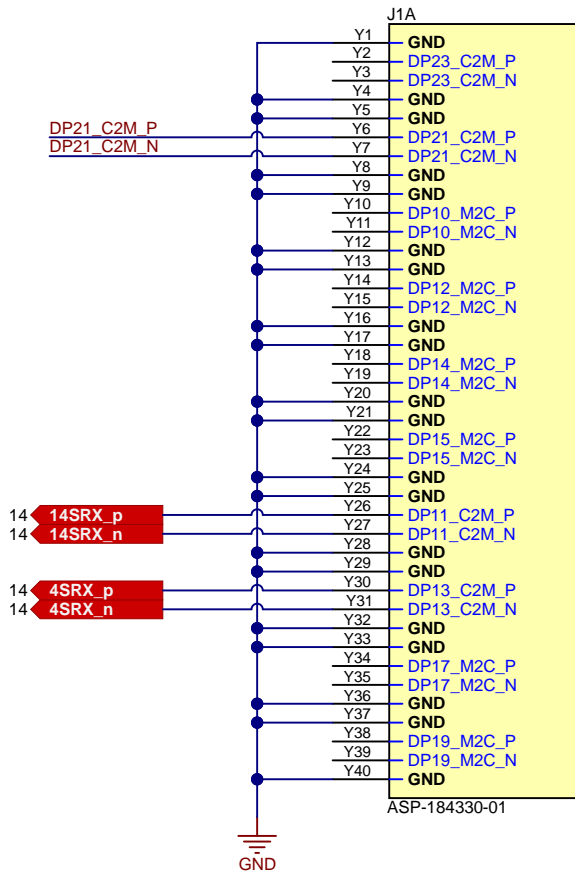
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### FMC+ Section Rows F - H, J, K



FMC+ Section Rows L, M, Y & Z

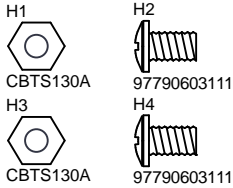


VITA SPEC or TSW14J59 compatible FMC+ connection

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Orderable: <a href="#">ChangeMe in variant</a>	Designed for: Public Release	Mod. Date: 1/24/2025
TID #: N/A	Project Title: DAC39RF20EVM	
Number: DC363	Rev: E1	Sheet Title: FMC+ Section Rows L, M, Y & Z
SVN Rev: e25fa76b6baa0590a0ec0a4d1b409015 [Locally Modified]	Sheet: 19 of 21	
Drawn By: <a href="#">Add comment</a>	File: FMC+ Sections Y, Z, L, M.SchDoc	Size: B
Engineer: MK	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	

Hardware & Mechanicals



PCB Number: DC363

PCB Rev: E1



PCB

LOGO

FCC disclaimer



CAUTION HOT SURFACE



LBL1

PCB Label

THT-14-423-10

Size: 0.65"x0.20"

ZZ1

Assembly Note

These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

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SVN Rev: 093cb5ca7a95023ded1b0a81110474b1020d1 [Locally Modified]		Sheet: <a href="#">20</a> of <a href="#">21</a>	
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Engineer: <a href="#">MK</a>		Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	

Rev History & Variants

Revision History

Rev	Release Date	Notes
E1	June-2024	Initial Release

Variant(s)

Variant	Notes
001	Original DNI components Used for production build
002	

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